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Stylesheet Version v1.1.1

Description

[METHOD FOR FABRICATING A NON-VOLATILE MEMORY AND METAL INTERCONNECT PROCESS]

Cross Reference to Related Applications

[0001] This application claims the priority benefit of Taiwan application serial no. 92136489, filed December 23, 2003.

Background of Invention

[0002] Field of the Invention

[0003] This invention generally relates to a method for fabricating a semiconductor device, and more particularly to a method for fabricating a non-volatile memory and a metal interconnect process.

[0004] Description of Related Art

[0005] Non-volatile memory devices have been used to store data. Flash memory is one type of the non-volatile memory devices, which is an electrically erasable programmable read only memory (EEPROM) in which data is

retained even after all power sources have been disconnected. Flash memory has been widely used in personal computers and other electronic equipment because it can provide the property of multiple entries, retrievals and erasures of data.

[0006] A conventional flash memory cell is a transistor with a control gate, a doped polysilicon floating gate and an oxide layer separating these two gates from each other. A tunneling oxide layer separates the floating gate and the substrate. During the programming of the memory, proper biases are applied to the source region, the drain region and the control gate. Electrons would then travel from the source region to the drain region through the channel. During this process, some of the electrons are injected through the tunneling oxide layer into the polysilicon floating gate, and the electrons are evenly distributed in the entire polysilicon floating gate. The injection of electrons into the polysilicon floating gate is known as the tunneling effect. The operation mechanism of a flash memory device includes the channel hot electron injection for programming of data and the Fowler-Nordheim Tunneling for the erasing of data. However, if defects are present in the tunneling oxide layer under-

neath the polysilicon floating gate, current leakage easily occurs, which affects the reliability of the memory device.

[0007] To prevent the flash memory from the current leakage problem, a charge-trapping layer has been proposed to replace the polysilicon floating gate, and the EEPROM is formed with a stacked gate structure comprising a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer. The material of the charge-trapping layer is silicon nitride. Hence, this kind of EEPROM is also called silicon nitride read only memory (NROM). Because the silicon nitride layer can trap charges, the injected electrons will not be distributed uniformly in the silicon nitride layer but Gaussian-distributed in the silicon nitride layer. Therefore, the current leakage will be reduced because most of the electrons are localized in small section of the silicon nitride layer, and thus they are insensitive to the defect of the tunneling oxide layer.

[0008] Another advantage of using silicon nitride layer is that during the programming process the electrons are stored locally in the channel, close to the source side or the drain side. Hence, during the programming process, the voltage can be applied to the source region and the control gate in one end of the stacked gate, and the Gaussian-dis-

tributed electrons are store in the silicon nitride layer at the drain region in the other end of the stacked gate, and. The voltage can also be applied to the drain region and the control gate in one end of the stacked gate, and the Gaussian-distributed electrons are stored in the silicon nitride layer at the source region in the other end of the stacked gate. Therefore, by changing the voltages applied to the control gates and the above two regions, there may be two groups of Gaussian-distributed electrons, one group of Gaussian-distributed electrons, or no electrons in a single silicon nitride layer. Hence, the flash memory using a silicon nitride layer to replace the floating gate can be programmed in four states, and such a memory cell is a two bits in one cell flash memory cell.

[0009] However, during the fabrication of the NROM, for example, in the PECVD process, the plasma causes the charges to move along the metal, which induces the so-called antenna effect. Hence, in a brief moment, a portion of electrons is trapped in the composite ONO layer such that a wide threshold voltage distribution among memory devices is resulted.

[0010] It should be noted that in addition to the antenna effect that leads to a wide threshold voltage distribution, the

clustering of the electrons on the surface of the film may result. For example, during the metal interconnect process of the NROM, an insulating layer is formed by the PECVD process to cover the metal lines. The material of the insulating layer is oxide or nitride. However, the plasma used in the PECVD process often causes a clustering of charges on the surface of the insulating layer. These charges then move to the silicon nitride layer in the ONO layer along the metal lines. As a result, a wide threshold voltage distribution among memory devices is resulted.

[0011] Further, during the photolithography process, an ultraviolet light is used for exposure. However, in a NROM device, electron-hole pairs are generated in the silicon nitride layer as the silicon nitride layer of the ONO layer being irradiated by the ultraviolet light. Further, because the holes are easily slipped away and only the electrons are left in the silicon nitride layer. Ultimately, a wide threshold voltage distribution among memory devices is resulted.

SUMMARY OF INVENTION

[0012] An object of the present invention is to provide a method for fabricating a non-volatile memory, wherein the antenna effect is mitigated to thereby prevent a wide thresh-

old voltage distribution among memory devices.

[0013] Another object of the present invention is to provide a method for fabricating a non-volatile memory to prevent the silicon nitride layer of the ONO layer from being exposed to the ultraviolet light, and the clustering of electrons in the silicon nitride layer.

[0014] Still another object of the present invention is to provide a metal interconnect process to reduce the amount of electrons clustering on the surface of the insolating layer formed by the PECVD process.

[0015] The present invention provides a method for fabricating a non-volatile memory, comprising first sequentially forming a tunneling layer, a trapping layer, a barrier layer, a gate conductive layer, and an anti-reflection layer on a substrate. Then, a photoresist layer with a pattern is formed the anti-reflection layer. The photoresist layer is used as an etching mask to pattern the anti-reflection layer, the gate conductive layer, the barrier layer, the trapping layer, and the tunneling layer, so as to form a stacked structure having the gate conductive layer, the barrier layer, the trapping layer, and the tunneling layer. This stacked structure is covered by the anti-reflection layer.

[0016] After removing the photoresist layer, a thin oxide layer is formed on the exposed surface of a control gate at the sidewalls. An insulating spacer is formed on each side sidewall of the stacked structure and covers the thin oxide layer. Then, a lining layer, which is used to resist ultraviolet light, is formed over the stacked structure, so as to prevent the ultraviolet light from entering to the trapping layer, and the causing charge accumulation on the trapping layer.

[0017] The present invention provides a fabrication process for metal interconnects, comprising: providing a substrate, the substrate having a conducting structure; forming a dielectric layer on the substrate to cover the conducting structure; forming a contact window in the dielectric layer, the contact window being electrically connected to the conducting structure; forming a conducting line structure on the dielectric layer, the conducting line structure being electrically connected to the contact window; and forming a low surface charge lining layer on the surfaces of the dielectric layer and the conducting line structure.

[0018] The present invention provides a method for fabricating a non-volatile memory, comprising first sequentially forming a tunneling layer, a trapping layer, a barrier layer, a

gate conductive layer, and an anti-reflection layer on a substrate. Then, a photoresist layer with a pattern is formed the anti-reflection layer. The photoresist layer is used as an etching mask to pattern the anti-reflection layer, the gate conductive layer, the barrier layer, the trapping layer, and the tunneling layer, so as to form a stacked structure having the gate conductive layer, the barrier layer, the trapping layer, and the tunneling layer. Wherein, the anti-reflection layer covers on top.

[0019] Then, after removing the photoresist layer, a thin oxide layer is formed in the exposed surface of the control gate. A spacer is formed on each sidewall of the stacked structure and also covers the thin oxide layer. Then, an ultraviolet-resistant lining layer is formed over the stacked structure, so as to prevent the ultraviolet light from entering to the trapping layer, and the causing charge accumulation on the trapping layer. A dielectric layer is formed on the ultraviolet-resistant lining layer. A contact window is formed in the dielectric layer, the contact window being electrically connected to the control gate. A conducting line structure is formed on the dielectric layer, the conducting line structure being electrically connected to the contact window. A lining layer with low surface charges is

formed on the surfaces of the dielectric layer and the conducting line structure.

[0020] In brief, the present invention, after forming the insulating spacer on the sidewall of the stacked structure, an ultraviolet-resistant lining layer is formed on the insulating spacer and the surface of the substrate to prevent the ultraviolet light from penetrating into the trapping layer, thereby reducing the amount of the electrons in the trapping layer. Further, the present invention can change the parameter of the PECVD process to form a low surface charge lining layer, thereby reducing the antenna effect.

[0021] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0022] FIGs. 1A-1G are cross-sectional views showing the progression of steps for fabricating a non-volatile memory in accordance with an embodiment of the present invention.

[0023] FIGs. 2A-2E are cross-sectional views showing the progression of steps for fabricating a non-volatile memory in accordance with another embodiment of the present invention.

[0024] FIGs. 3A-3D are cross-sectional views showing the progression of steps for fabricating the metal interconnect process in accordance with the present invention.

DETAILED DESCRIPTION

[0025] FIGs. 1A-1G are cross-sectional views showing the progression of steps for fabricating a non-volatile memory in accordance with an embodiment of the present invention. Referring to FIG. 1A, a tunneling layer 102, a trapping layer 104 and barrier layer 106 are sequentially formed on a substrate 102. The material of the substrate 100 is,for example, silicon; the barrier layer 102 is, for example, a silicon oxide layer. The trapping layer 104 is, for example, a silicon nitride layer. The barrier layer 106 is, for example, a silicon oxide layer.

[0026] A polysilicon layer 108 and a metal silicide layer 107 are sequentially formed on the barrier layer 106, wherein the polysilicon layer 108 and the metal silicide layer 107 form a gate conductive layer 105. An anti-reflection layer 110 is formed on the gate conductive layer 105. Wherein, the polysilicon layer 108 is formed by a method including, for example, a chemical vapor deposition. The metal silicide layer is formed by a method including, for example, forming a metal layer on the polysilicon layer 108, and per-

forming a thermal process to cause a reaction between the metal layer and the polysilicon layer 108, so as to form the metal silicide layer 107. A photoresist layer 112 with a pattern is formed n the anti-reflection layer 110 by the photolithographic processes.

[0027] Referring to FIG. 1B, using the photoresist layer as the etching mask to perform etching process, the tunneling layer 102, the trapping layer 104, the barrier layer 106, the gate conductive layer 105, and the antireflection layer 110 are patterned to form a stacked structure 113, which includes the tunneling layer 102a, the trapping layer 104a, the barrier layer 106a (oxide/nitride/oxide composite layer), and the gate conductive layer 105a. The stacked structure 113 is covered by the anti-reflection layer 110a.

[0028] In the foregoing photolithographic process on the photoresist layer, the anti-reflection layer 110 can absorb light, so that the exposing light source is prevented an interference between the incident light and the reflected light from the substrate or the film layer. Also and, the anti-reflection layer 110 includes, for example, organic or inorganic dielectric materials. If the anti-reflection layer 110 includes the inorganic dielectric material, the fabrica-

tion processes are following.

[0029] In FIG. 1C, after the photoresist layer 112 is removed, since the anti-reflection layer 110a includes the inorganic dielectric material, the anti-reflection layer 110a is not removed while removing photoresist layer 112. Then, then exposed surface of the control gate 105a, that is, the surface at the sidewalls of the control gate 105a, is formed with a thin oxide layer 119. In one embodiment, the thin oxide layer 119 is formed, for example, by a thermal oxidation process, wherein the oxygen and nitrogen gases are flowed through. Here, the thin oxide layer 119 and the anti-reflection layer 110a can be used to protect the control gate 105a form being damaged by the subsequent fabrication process.

[0030] In FIG. 1D, a source/drain region 114 is formed in the substrate 10 at each side of the control gate 105a. An insulating spacer 116 is formed on each side of the stacked structure 113. The spacer 116 can be formed by, for example, forming a dielectric layer (not shown) over the substrate 100 by, for example, chemical vapor deposition (CVD), and performing an etching back process on the dielectric layer, so as to form the spacer 116. The dielectric layer includes, for example, silicon oxide.

[0031] Referring to FIG. 1E, a plasma enhanced CVD (PECVD) is performed to form an ultraviolet-resistant lining layer 118 on the surfaces of the substrate 100 and the spacer 116. In a preferred embodiment of the present invention, the material of the ultraviolet-resistant lining layer 118 is silicon nitride, for example. The process parameters for forming the ultraviolet-resistant lining layer 118 are as follows. The reacting gas includes a silane (SiH_4) gas with a flow rate between 50sccm and 60sccm, preferably 55sccm, an ammonium (NH_3) gas with a flow rate between 20sccm and 30sccm, preferably 25sccm, and a nitrogen (N_2) gas with a flow rate between 2600sccm and 3000sccm, preferably 2800sccm. The temperature for the PECVD process is between 380°C and 420°C, preferably 400°C; the power for the PECVD process is between 370W and 410W, preferably 390W; the pressure for the PECVD process is between 7.0 torr and 8.0 torr, preferably 7.5 torr. The thickness of the film is between 180Å and 220Å, preferably 200Å. It should be noted that the flow rates of SiH_4 and NH_3 and the applied power are smaller than those in the conventional method. Hence, the thin film formed under those parameters is much denser because of a lower deposition rate.

[0032] Taking the ultraviolet-resistant lining layer 118 as an example, the deposition rate for the ultraviolet-resistant lining layer 118 of the present invention is 680 Å per minute, which is much lower than the conventional deposition rate 7000 Å per minute. Hence, the ultraviolet-resistant lining layer 118 formed under those parameters is much denser. Therefore, during the subsequent photolithography process, the ultraviolet-resistant lining layer 118 can effectively prevent the ultraviolet light from penetrating into the trapping layer 104 so that the unwanted clustering charges in the trapping layer 104a is prevented. Further, even if the charges may be clustered in the ultraviolet-resistant lining layer 118 due to the exposure to the ultraviolet light, the trapping layer 104a is not affected because there is an insulating spacer 116a between the ultraviolet-resistant lining layer 118 and the trapping layer 104a.

[0033] In another preferred embodiment of the present invention, a metal interconnect process is performed subsequent to the process step as shown in FIG. 1E. First, in FIG. 1F, an inter-layer dielectric (ILD) material 120 is formed on the ultraviolet-resistant lining layer 118. Then, a contact 122 is formed in the inter-layer dielectric mate-

rial 120 through the ultraviolet-resistant lining layer 118 and the patterned anti-reflection layer 110a. Thereafter, a metal layer 26 is formed on the dielectric layer 120 and the contact 122.

[0034] Referring to FIG. 1G, photolithography and etching processes are performed to pattern the metal layer 126 to form a conducting line structure 126a. The conducting line structure 126a is electrically connected to the control gate 105a via the contact window 122. Then, the PECVD process is performed to form a low surface charge lining layer 128 on the surfaces of the conducting line structure 126a and the inter-layer dielectric material 120. The material of the low surface charge lining layer 128 can be silicon oxide or silicon nitride. Taking silicon oxide as an example, the process parameters for forming the low surface charge lining layer 128 are as follows. The reacting gas includes SiH_4 with a flow rate between 20sccm and 30sccm, preferably 25sccm, and N_2O with a flow rate between 750sccm and 1000sccm, preferably 900scc. The temperature for the PECVD process is between 380°C and 420°C, preferably 400°C. The power for the PECVD process is between 370W and 410W, preferably 390W. The pressure for the PECVD process is between 2.0 torr and

3.0 torr, preferably 2.5 torr. The thickness of the film is between 900Å and 3300Å, preferably about 2000Å. It should be noted that the flow rate of SiH_4 and the applied power are smaller than those of the conventional method. Hence, the thin film formed under those parameters is much denser because of a lower deposition rate. For example, the deposition rate is reduced from 12000Å per minute to 3800Å per minute.

[0035] It should be noted that when the film is formed by the PECVD process, the accumulated charges and the charge distribution depend on the reacting gas and the power applied in the process. In the conventional PECVD process, the power applied to form a silicon oxide layer is 185W and the flow rate of SiH_4 is 90sccm. However, in the embodiments of the present invention, the power and the flow rate of SiH_4 is much lower than those in the convention PECVD. Hence, the parameters in the embodiments of the present invention can reduce the charges being clustered on the surface of the lining layer 128, thereby reducing the antenna effect. Further, if the material of the low surface charge lining layer 128 is, for example, silicon nitride, the low surface charge lining layer 128 can also prevent the penetration of moisture into the device.

[0036] In this embodiment, the amount of charges in the low surface charge lining layer 128 are determined by measuring the work functions of the low surface charge lining layer 128 and the substrate 100. If there is a big difference between those two work functions, it is an indication that there are more charges in the low surface charge lining layer 128, and vice versa. By measuring the work functions, whether the low surface charge lining layer 128 meets the low surface charge requirement can be determined.

[0037] In addition, in another embodiment of the invention, the anti-reflection layer 110a is formed form an organic material. In this manner, after the stacked structure 113 (such as FIG. 1B) is patterned, the photoresist layer is removed to expose the control gate 105a, as shown in FIG. 2A. Here, since the anti-reflection layer is formed by organic material, during removing the photoresist layer 112, the anti-reflection layer 110a is removed at the same time. Then, the exposed surface of the control gate 105a is formed with a thin oxide layer 119a., wherein the thin oxide layer is formed, for example, on top and side walls of the control gate 105a. The thin oxide layer 119a is used to protect the control gate 105a from being dam-

aged from subsequent fabrication processes. The thin oxide layer 119a is similar to the thin oxide layer 119 in material and fabrication method.

[0038] And, the like numerals represent the like elements. The material and the fabrication method are similar to the previous embodiment without further descriptions.

[0039] In FIG. 2B, the source/drain region 114 is formed in the substrate 100 at each side of the stacked structure 113. An insulating spacer 116 is formed on the sidewalls of the stacked structure 113 and covers the thin oxide layer 119a on the sidewalls of the control gate 105a.

[0040] In FIG. 2C, a PECVD process is performed to form an ultraviolet-resistant lining layer 118 over the spacer 116 and the substrate 100. In FIG. 2D, an inter-layer dielectric layer 120 is formed on the ultraviolet-resistant lining layer 118. A contact window 122 is formed in the inter-layer dielectric layer 120 and penetrates the ultraviolet-resistant lining layer 118 and the thin oxide layer 119a on the control gate 105a. Then, a metal layer 126 is formed on the dielectric layer 120 and the contact window 122.

[0041] In FIG. 2E, the metal layer 126 is patterned by photolithographic and etching processes to form, for example, a patterned conductive structure 126a. The conductive

structures 126a is electrically coupled to the control gate 105a by the control window 122. A PECVD process is performed to form a lining layer 128 with low surface charges on the conductive structures 126a and the dielectric layer 120.

[0042] The application of the metal interconnect process in the above embodiment is not limited to the non-volatile memory. It also can be applied to other metal interconnect process. Another embodiment of the present invention is described as follows. Referring to FIG. 3A, a substrate 300 is provided; the substrate 300 includes a conducting structure 302, such as, a MOS transistor. Referring to FIG. 3B, a dielectric layer 306 is formed on the surface of the substrate 300 and the conducting structure 302. Then, a contact 308 is formed in the dielectric layer 306. Referring to FIG. 3C, a metal layer 312 is then formed on the top surfaces of the dielectric layer 306 and the contract 308.

[0043] Referring to FIG. 3D, an etching process is performed to pattern the metal layer 312 thereby forming a conducting line structure 312a electrically connected to the contact window. Then, the PECVD process is performed to form a low surface charge lining layer 314 on the surfaces of the conducting line structure 312a and the dielectric layer

306. The material of the low surface charge lining layer 314 can be silicon oxide or silicon nitride. Taking silicon oxide as an example, the process parameters for forming the low surface charge lining layer 314 are as follow. The reacting gas includes SiH_4 with a flow rate between 20sccm and 30sccm, preferably 25 sccm, and N_2O with a flow rate between 350 sccm and 1000sccm, preferably 900sccm. The temperature for thePECVD process is between 380°C and 420°C, preferably 400°C. The power for the PECVD process is between 370W and 410W, preferably 390W. The pressure for PECVD is between 2.0 torr and 3.0 torr, preferably 2.5 torr. The thickness of the film is between 900Å and 3300Å, preferably 2000Å.

[0044] In brief, the present invention uses a PECVD process, which is conducted with a lower power and a low deposition rate to form a denser and a lower surface charge lining layer to thereby mitigate the antenna effect. Further, the present invention uses a PECVD process, which is conducted with a lower power and a low deposition rate to form the ultraviolet-resistant lining layer to prevent the ultraviolet light from penetrating into the trapping layer and to prevent the unwanted charges from being trapped by the trapping layer. Because the method for fabricating

a non-volatile memory and the metal interconnect process of the present invention are very simple, the objects of the present invention can be achieved without further complicating the process.

[0045] The above description provides a full and complete description of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.